REMARKS

Reconsideration and allowance of this application, as amended, are respectfully requested.

Formalities

The formal drawings will be amended to include the labels 'Prior Art' where suggested by the Examiner. The ABSTRACT OF THE DISCLOSURE has been rewritten as required by the Examiner. The claims have been amended keeping in mind the Examiner's 35 USC 112 rejections.

The prior art rejections are respectfully traversed. Various of the claims are amended to even more clearly point out differences between the claimed inventions and the prior art references.

Our claimed inventions

Our claimed inventions, in general, relate to using a high pixel rate imaging element with a Bayer array filter. Same color line addition read-out is executed without increasing the drive clock frequency of imaging elements so as not to reduce the frame rate of image signal for AE, AWB and AF controls. We focus on thin out read-out.

Our claim 14 arrangement can be set, in addition to a full pixel read-out mode, to a same color thin-out read-out mode, in which k ($k \geq 6$, k being an integral number) lines of a pixel signal obtained by adding together, in a vertical register, n ($n \geq 2$, n being an integral number) lines for every in ($m \geq 3$, m being an integral number) vertical lines of a solid-state imaging element are partly taken out.

With this construction and arrangement, the same color thin-out read-out mode is adopted in the case of using the high pixel imaging element having a Bayer array filter. By so doing, the frame rate of the image signal for the AE, AWB and AE controls is not reduced, and imaging time lag increase is prevented.

Our claim 15 arrangement can be set, in addition to a full pixel read out mode, to a thin-out read-out mode, in which n ($n \geq 2$, n being an integral number) lines are added together in a vertical register are taken out from the solid-state imaging element for every m ($m \geq 3$, m being an integral number) vertical lines, as well as the same color thin-out read-out mode, n which k ($k \geq 6$, k being an integral number) lines of the pixel signal obtained by adding together n lines for every m vertical lines of the solid-state imaging element are partly taken out.

With this construction and arrangement, the same color thin-out read-out mode is adopted in the case of using the high pixel rate imaging element. By so doing the frame rate of the image signal for the AE, AWB and AE controls is not reduced, and the imaging time lag increase is prevented.

Claims 14, 16, 17, 18 and 22-23

Claims 14, 16, 17, 18 and 22-23 stand rejected under 35 USC 102(e) as being anticipated by Parulski et al ('406). This ground of rejection is respectfully traversed. Furthermore, the claims, as amended are believed to be non-obvious under 35 USC 103 with respect to this reference.

Parulski et al ('406) show an electronic camera having a preview mode and a still mode in which image data of an image sensor are fitted to the number of pixels in a color

LCD. A thin-out read out is carried out in the preview mode. This camera is designed for conversion of an aspect ratio between an imaging element and an LCD display element. At the same time of the thin-out read-out the same color line addition is executed by using a horizontal register added for the addition operation.

The Examiner expresses concern in middle portion of page 5 of the Office Action relating to the TFT type LCD shown in Fig. 1. In Applicant's view, this is irrelevant to our imaging element. Circuit 32 is constituted by a correlated double sampling circuit and an amplifier, and does not function to combine a thin-out read-out signal. As an extra example shown in Paruiski et al ('409) a pixel re-mapper 62 rearranges thin-out read-out lines for LCD display. The reference fails to discloses the same color line thin-out addition mode as we claim. According Perulaki et al ('405) a line-skipping read-out mode (Fig. 7), although supporting the dynamic picture image mode, is for line addition by using a separate horizontal register. Therefore, this mode is irrelevant to the same color addition thin-out read-out mode utilizing the vertical register as we claim. Thus, Applicant respectfully requests that the rejection of claim 14 be withdrawn. As noted above, the rejection of claim 14 appears to be improper and the rejection of its dependent claims should also be withdrawn.

Claims 19-21

Claims 19-21 stand rejected under 35 USC 103 as being unpatentable over Parulski ('406) in view of Whipple et al. This ground of rejection is respectfully traversed.

Whippel et al disclose execution of same color line addition by using a horizontal register provided for the addition operation. Thus, even combining the Whippel et al teachings with those of Parulski '406 does not result in the combinations defined by claims 19-21, as amended.

Claims 15 and 24

Claims 15 and 24 stand rejected under 35 USC 103 as being unpatentable over Terada et al in view of Parulski '597. This ground of rejection is respectfully traversed.

Paruiski et al ('597) disclose the execution, at the time of thin-out read-out, of same color line addition by using a horizontal register provided for the addition operation.

Terade et al teach a technique of same color pixel addition at the time of thin-out read-out by using a solid-state imaging element capable of non-destructive read-out in XY address (random access) control system and a line memory provided in a vertical/horizontal scanning circuit in the imaging element.

The imaging element according to Terade is a non-destructive read-out type imaging element (CMD) in an XV address i.e. random access control system. Thus, this imaging element is based on the progressive read-out system, and is irrelevant in the drive principle to the non-destructive read-out type CCD. Our claim 15 arrangement is not obvious from the teachings of these two references, even combined.

In view of the above, a Notice of Allowance for the claims, as amended, is respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned "Version with markings to show changes made".

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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Enclosures: Appendix
Abstract
Drawing Corrections Approval Request (Incl. Figs. 24-26)

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as follows:

14. (Amended) An electronic imaging system comprising:

a solid-state image sensor having a two-dimensional array of pixels capable of converting light incident thereon to electric signal, the pixels being arranged in a plurality of horizontal lines, the lines being arranged vertically one under another; [and]

a color filter arranged on a incident plane of the solid-state image sensor having a line sequential mosaic pattern; and

control means for selectively controlling a mode for sequential scan reading out pixel signals concerning the whole pixels of the solid-state image sensor for still picture recording, and a mode for reading out pixel signal sums by utilizing a plurality of vertical registers each of n ($n \geq 2$, n being an integer) lines among m ($m \geq 3$, m being an integer) lines in k ($k \geq 6$, k being an integer) continuous lines of the solid-state image sensor for still picture recording or dynamic image processing.

15. (Amended) An electronic imaging system comprising:

a solid-state image sensor having a two-dimensional array of pixels capable of converting light incident thereon to electric signal, the pixels being arranged in a plurality of horizontal lines, the lines being arranged vertically one under another ; [and]

a color filter arranged on a incident plane of the solid-state image sensor having a line sequential mosaic pattern ; and

control means for selectively controlling a mode for sequential scan reading out pixel signals concerning the whole pixels of the solid-state image sensor for still picture recording, a mode for reading out pixel signal sums by utilizing a plurality of vertical registers each of n ($n \geq 2$, n being an integer) lines among m ($m \geq 3$, m being an integer) lines of the solid-state image sensor for still picture recording or dynamic image processing, and a mode for reading out pixel signal sums by utilizing a plurality of vertical registers of n lines among m lines in k ($k \geq 6$, k being an integer) partially continuous lines of the solid-state image sensor for still picture recording or dynamic image processing.

16. (Amended) The electronic imaging system as set forth in claim 14 or 15, in which the control means controls a mode of reading a plurality of k line blocks each of k lines in the whole lines for said still picture recording or dynamic image processing.

17. (Amended) The electronic imaging system as set forth in claim 14, 15 or 16 in which image data obtained by reading out said pixel signal sums each of n lines among m vertically continuous lines for still picture recording or dynamic image processing, is such that its color signal is line sequential data.

22. (Amended) The electronic imaging system as set forth in claim 14, 15 or 16, in which dynamic image processed signal obtained in either of the [above] modes is used for AF, AE or AWB control data.

23. (Amended) The electronic imaging system as set forth in claim 14, 15 or 16, in which dynamic image processed signal obtained in either of the [above] modes is used as AF, AE or AWB control data, and the AF, AE [and] or AWB control data [being] is calculated sequentially each in each frame.

24. (Amended) The electronic imaging system as set forth in claim 15, in which the control means selects a mode of reading out pixel signal sums each of n lines among m vertically continuous lines when obtaining dynamic image processed signal to be displayed on a display provided in [it], the system to be supplied to an external display provided outside [it] the system or to be used as AE or AWB control data, and the control means selects a mode of reading out pixel signals of n lines among every m vertically continuous lines in k partially continuous lines when obtaining dynamic image processed signal to be used as AF or AE control data.